REMARKS

Statement of Substance of Interview

Applicants thank Examiner Flores for a very helpful telephonic interview with Mr. Hurley and the undersigned, conducted January 22, 2008. The above amendments and following remarks were presented. Prior approaches and problems described in the background section of the disclosure were discussed, and, in particular, the desire to reduce the length of a delay chain after initial synchronization and how to skip registers while avoiding the problem of losing data samples by tapping a register too far back in the chain. With reference to FIG. 5, Applicants' technique of shifting data samples out of a clocked delay chain at a higher output rate than data samples coming into the clocked delay chain was also reviewed. Applicants further discussed how the cited Alexander reference deals with clock edges, does not receive a sequence of data, is not a clocked delay chain, and how its propagation delay is based on the physical medium of which the delay units are made (i.e. distance traveled). Examiner Flores indicated he would require further review, so it was agreed Applicants would file an RCE, and if not allowed, any further action would not be final.

Rejection under 35 U.S.C. 103(a)

Claims 1-20 are pending in this application.

The title is being amended to indicate more clearly the invention to which the claims are directed. The specification is also being amended to correct a typographical error. Support for this amendment may be found at least in FIG. 2 and on page 5, lines 9 through 12 of the specification as originally filed.

Claims 1-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art (hereinafter "Prior art") in view of US Patent 6,765,419 B2 by Alexander (hereinafter "Alexander").

Without limitation of the claims, the disclosed embodiments pertain to digital processing of discrete data samples and to data path latency due to processing of samples through delay chains. Delay chains are used within digital systems to allow for various processing events, such as timing recovery of the samples' boundaries. For example, a number of initial data samples may be collected in a delay chain to be processed together. Subsequent data samples need not be

processed but continue to follow through the delay chain. The processing of samples through such a delay chain subsequent to the processing event that required the delay chain, may unnecessarily add to the data path latency and, consequently, lead to suboptimal performance. Disclosed embodiments provide for reduction of the data path latency by dynamically reducing the length of a given delay chain after completion of a processing event. In particular, the length of a given delay chain may be effectively reduced by shifting samples out of the delay chain faster than the rate at which new data samples are read into the delay chain and then bypassing empty delay elements of the delay chain.

FIG. 5 depicts an example embodiment illustrating a technique of shifting data samples out of a clocked delay chain faster than the rate at which new data samples are shifted into the clocked delay chain. As shown in clock cycles 1 and 2, data samples (shown as a "+") propagate through the delay chain such that each contiguous register stores a data sample. At clock cycle 3, an event (e.g., timing recovery completion) causes the delay chain to enter a "FAST mode." In this mode, output data samples are clocked out every clock cycle as shown in the upper right-hand region in FIG. 5, and input data samples are simultaneously clocked into the delay chain once every four clock cycles as shown in the lower left region of FIG. 5. As can be seen, the difference in data rates results in a number of contiguous empty registers that ultimately extend to the output. At that time, an earlier register can be tapped for the output, bypassing the empty registers and reducing the length of the delay chain for all subsequent data. The process can be repeated to further shorten the delay chain.

Thus, in the example embodiment, processing data samples includes "shifting data samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain, and dynamically reducing the length of the clocked delay chain as data samples continue to be read into the clocked delay chain" as claimed in amended Claim 1. Support for this amendment may be found at least on page 5, lines 19-23 and page 9, lines 3-10 of the specification as originally filed.

Applicants continue to maintain that Alexander is non-analogous art, as indicated in the previously filed amendment and as discussed below. Alexander pertains to an analog delay locked loop (DLL) meant to control edge skew of clock signals through the use of delay units/blocks. Clock signals are delayed based on the amount of time it takes the signal to

propagate though the physical medium of which the delay units are made, therefore, distance traveled.

In contrast, Applicants disclose a method of processing data samples from a clocked delay chain. The data samples are stored and clocked through the delay chain at a speed directly proportional to the clock frequency of the digital circuit. Since the clock frequency of the digital circuit is not generally proportional to the propagation delay of the signal through the delay units, movement of the discrete data samples through the digital delay chain is not generally proportional to the speed at which the signal propagates through the delay units. To further clarify this distinction, Claims 1, 2, 5-8, and 14-16 have been amended to recite "data samples" and a "clocked delay chain."

Accordingly, Applicants maintain that Alexander is from a different art than the Prior art and combining the two references would not be obvious. Furthermore, even if Alexander and the prior art were combined, Applicants believe the combination does not teach, suggest, or make obvious the invention of Claim 1 as discussed below.

FIG. 1 in Alexander discloses a delay lock loop (DLL) circuit 10 that is used to align clock edges. The delay circuit does not receive a sequence of data samples, and there is no processing of data samples from taps on the delay. The circuit 10 compares a reference clock signal 22 to a feedback clock signal 24 and generates an output clock signal 26 by delaying the reference clock signal 22 via a forward delay circuit 12. The comparison and delay are iterated until the feedback clock 24 is aligned in time with the reference clock signal 22. (See column 3, lines 33-40.) A control signal 28 is used to increase, decrease or leave unchanged the amount of time by which the output clock signal 26 is delayed relative to the reference clock signal 22. (See column 4, lines 2024, and column 6, lines 8-18.) Thus, the output clock edge may be increased, decreased, or left unchanged relative to the input clock edge. However, the output clock signal 26 operates at the same rate at which the input clock 22 operates. Alexander does not teach or suggest "shifting data samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain" as claimed in amended Claim 1 as recited above.

According, Applicants respectfully submit that Claim 1 is patentable over the cited references and is in condition for allowance.

Claims 2-7 depend directly or indirectly on Claim 1 with limitations to the features thereof. It is, thus, respectfully submitted that Claims 2-7 are also allowable.

Independent Claim 8 has been amended to recite similar elements . It is respectfully submitted that Claim 8 is allowable for at least the same reasons as indicated above.

Independent Claims 9 and 13 recite in part "a processor ... which controls the data shifting rates, the logic circuitry, and the output of the multiplexer based on a plurality of processing events of the apparatus." Neither Alexander nor the Prior Art teach, suggest or make obvious a processor which controls the data shifting rates. It is, thus, respectfully submitted that Claims 9 and 13 are also allowable. Claims 9 and 13 have also been amended to recite "logic circuitry which controls ~~the output of~~ each individual register ~~from~~ of the pipeline of registers ..." to more clearly define the invention as described in the application as originally filed. Support for this amendment may be found at least in FIG. 3 and in the specification on page 6, line 25 to page7, line 12.

Claims 10-12 depend directly or indirectly on Claim 9 with limitations to the features thereof. Claim 10 is a system claim analogous to Claim 2, Claim 11 is dependent on Claim 10, and Claim 12 is dependent on Claim 11. It is, thus, respectfully submitted that Claims 10-12 are also allowable.

Claims 14 and 15 have been amended to recite limitations similar to those in amended Claim 1. Applicants respectfully submit that amended Claims 14 and 15 are also allowable for at least the same reasons presented above.

Claims 16-20 recite limitations of Claims 1-15 in the same or equivalent language. In particular, Claims 16-18 depend directly or indirectly on Claim 15 with limitations to the features thereof. Claim 18 has also been amended to correct a typographical error. Claim 19 depends on independent Claim 9, and Claim 20 depends on independent Claim 13. It is, thus, respectfully submitted that Claims 15-20 are allowable for at least the same reasons discussed above with respect to Claims 1-15.

Therefore, because neither Alexander nor Applicants' prior art, taken alone or in combination, teach, suggest or make obvious the invention of Claims 1-20, Applicants respectfully submit that Claims 1-20 are patentable over the cited references.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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